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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/645,645	MOULI, CHANDRA	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/21/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of group I, claims 1-37, in the reply filed on 10/05/04 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5-8, 11-13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,818,322 to Tasumi in view of US Patent No. 6,587,142 to Kozlowski et al.

Regarding claim 1, Tasumi (figures 1a-c) teaches a pixel cell for an image sensor, the pixel cell comprising:

a photodiode (superlattice structure [6]) for generating charge in response to light and for amplifying the generated charge, the photodiode (superlattice structure [6]) being over a surface of a substrate (1) and comprising a plurality of layers (superlattice structure [6] comprises a plurality of layers).

Tasumi teaches the first layer and second layer (superlattice structure [6] comprises alternating layers of Si and SiGe), which are Si and SiGe, the same material as the instant

invention. Therefore, the first layer and second layer of Tasumi have a first band gap and a second band gap, which separate the energy between the first layer and the second layer.

Tasumi teaches the device (3) (driver; column 5, lines 43-46), which is adjacent to the photodiode (superlattice structure [6]). Tasumi differs from the claimed invention by not showing a gate adjacent to the photodiode for transferring the amplified charge from the photodiode. However, Kozlowski et al. teach a photodiode (12), which is connected to the gate of a driver MOSFET (column 7, lines 4-11). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Kozlowski et al. into the device taught by Tasumi in order to transfer the signals of the photodiode to the external device. The combined device shows a gate adjacent to the photodiode for transferring the amplified charge from the photodiode.

Regarding claim 2, Tasumi teaches the first layer and second layer (superlattice structure [6] comprises alternating layers of Si and SiGe), which are Si and SiGe, the same material as the instant invention. Therefore, the first and second layers of Tasumi have a difference between the conduction band energies of the first layer and the second layer is greater than a difference between the valence band energies of the first layer and the second layer, which reduce the dark current and minimize the noise between the first layer and the second layer.

Regarding claim 3, Tasumi teaches the first layer and second layer (superlattice structure [6] comprises alternating layers of Si and SiGe), which are Si and SiGe, the same material as the instant invention. Therefore, the first and second layers of Tasumi have a difference between the valence band energies of the first layer and the second layer is greater than a difference between

the conduction band energies of the first layer and the a second layer, which suppress the impact of the ionization between the first and second material layer.

Regarding claim 5, the combined device shows the layers (Tasumi; superlattice structure [6] comprises Si) are each formed of a material selected from Si.

Regarding claim 6, the combined device shows the first layer is Si and the second layer is SiGe (Tasumi; superlattice structure [6] comprises alternating layers of Si and SiGe).

Regarding claim 7, the combined device shows the photodiode (Tasumi; superlattice structure [6]) comprises at least two layers of Si (Tasumi; 2 layers of Si of the superlattice structure [6]) and at least two layers of SiGe (Tasumi; 2 layers of SiGe of the superlattice structure [6]), wherein the layers of Si are doped to a first conductivity type, wherein the layers of SiGe are doped to a second conductivity type, and wherein the layers of Si are alternated with the layers of SiGe to form an Si/SiGe structure.

Regarding claim 8, the combined device shows the photodiode (Tasumi; superlattice structure [6]) comprises at least four layers of Si (Tasumi; 4 layers of Si of the superlattice structure [6]) and at least four layers of SiGe (Tasumi; 4 layers of SiGe of the superlattice structure [6]), wherein the layers of Si are alternated with the layers of SiGe to form an Si/SiGe structure, wherein at least a first subset of layers is doped to a first conductivity type, and wherein at least a second subset of layers is doped to a second conductivity type.

Regarding claim 11, the combined device shows at least a portion of the photodiode (Tasumi; a portion of superlattice structure [6] is below the top surface of the substrate [1]) is at a level below the level of a top surface of the substrate.

Regarding claim 12, the combined device shows the photodiode comprises approximately 10 to approximately 100 layers (Tasumi; superlattice structure [6] comprises 22 layers, which is in the range of the claimed invention).

Regarding claim 13, the combined device differs form the claimed invention by not showing each of the layers have a thickness of approximately 50 Angstroms to approximately 300 Angstroms. It would have been obvious to one having ordinary skill in the art at the time the invention was made for each of the layers have a thickness of approximately 50 Angstroms to approximately 300 Angstroms in order reduce the thickness of the device. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 19, the combined device shows the substrate (Tasumi; column 4, lines 19-22) is a silicon-on-insulator substrate.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tasumi in view of Kozlowski et al., and further in view of US Patent No. 6,127,692 to Sugawa et al.

Regarding claim 4, the disclosures of Tasumi and Kozlowski et al. are discussed as applied to claims 1-3, 5-8, 11-13 and 19 above.

The combined device differs from the claimed invention by not showing the layers are configured to promote ionization by a first carrier type and suppress ionization by a second carrier type. However, Sugawa et al. teach the layers are configured to promote and suppress ionization of the layers (column 21, lines 32-36). Therefore, it would have been obvious to one

having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sugawa et al. into the device taught by Tasumi and Kozlowski et al. in order to suppress the dark current in the layers.

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tasumi in view of Kozlowski et al., and further in view of US Patent No. 6,403,975 to Brunner et al.

Regarding claim 9, the disclosures of Tasumi and Kozlowski et al. are discussed as applied to claims 1-3, 5-8, 11-13 and 19 above.

The specification shows the value of x and y is $0 \leq (x \text{ or } y) \geq 1$ (page 10; paragraph [0046]). For instance, the value of $x = y = 0.5$, then the first layer of Si_xGe_{1-x} will be $Si_{0.5}Ge_{0.5}$ and the second layer of Si_yGe_{1-y} will be $Si_{0.5}Ge_{0.5}$.

The combined device differs from the claimed invention by not showing the first layer is Si_xGe_{1-x} (or $Si_{0.5}Ge_{0.5}$) and the second layer of Si_yGe_{1-y} (or $Si_{0.5}Ge_{0.5}$). However, Brunner et al. (figure 4c) teach the first layer of $Si_{1-x}Ge_x$ and the second layer of $Si_{1-x}Ge_x$ in the superlattice structure (alternating layers). Brunner et al. teach the value of x is in the range from 0.2 to 0.5 (column 8, lines 22-23), so the first layer of $Si_{1-x}Ge_x$ will be $Si_{0.5}Ge_{0.5}$ (when x is 0.5) and the second layer of $Si_{1-x}Ge_x$ will be $Si_{0.5}Ge_{0.5}$ (when x is 0.5). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Brunner et al. into the device taught by Tasumi and Kozlowski et al. in order to provide highly sensitive to a longer wavelength of the device.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tasumi in view of Kozlowski et al., and further in view of US Patent No. 6,403,975 to Brunner et al. and US Patent No. 5,557,121 to Kozuka et al.

Regarding claim 10, the disclosures of Tasumi and Kozlowski et al. are discussed as applied to claims 1-3, 5-8, 11-13 and 19 above.

The specification shows the value of x and y is $0 \leq (x \text{ or } y) \geq 1$ (page 10; paragraph [0046]). For instance, the value of $x = 0.5$ and $y = 0$, then the first layer of $Si_xGe_{1-x}C_y$ will be $Si_{0.5}Ge_{0.5}$

The combined device differs from the claimed invention by not showing the first layer is $Si_xGe_{1-x}C_y$ (or $Si_{0.5}Ge_{0.5}$). However, Brunner et al. (figure 3a) teach the first layer of $Si_{1-x-y}Ge_xC_y$ in the superlattice structure (alternating layers). Brunner et al. teach the value of x is in the range from 0 to 0.5 and y is in the range from 0 to 0.1 (column 8, lines 19-20), so the first layer of $Si_{1-x-y}Ge_xC_y$ will be $Si_{0.5}Ge_{0.5}$ (when $x = 0.5$ and $y = 0$). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Brunner et al. into the device taught by Tasumi and Kozlowski et al. in order to provide the long wavelength light of the device.

The combined device differs from the claimed invention by not showing the second layer is $Si_xGe_yC_z$. However, Kozuka et al. teach the layer of $Si_xGe_yC_z$ (column 5, lines 53-54). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Kozuka et al. into the device taught by Tasumi, Kozlowski et al. and Brunner et al. in order to provide the long wavelength light of the device.

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tasumi in view of Kozlowski et al., and further in view of US Patent No. 5,847,409 to Nakayama.

Regarding claim 14, the disclosures of Tasumi and Kozlowski et al. are discussed as applied to claims 1-3, 5-8, 11-13 and 19 above.

The combined device differs from the claimed invention by not showing a graded buffer layer between a bottom layer of the photodiode and a surface of the substrate. However, Nakayama (figure 2) teaches a graded buffer layer (102), which is formed on the substrate (101). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Nakayama into the device taught by Tasumi and Kozlowski et al. in order to reduce the strain between the upper layer and the surface of the substrate.

8. Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tasumi in view of Kozlowski et al., and further in view of US Patent No. 6,762,401 to Lee.

The disclosures of Tasumi and Kozlowski et al. are discussed as applied to claims 1-3, 5-8, 11-13 and 19 above.

Regarding claim 15, the combined device differs from the claimed invention by not showing the transistor is a reset transistor for resetting the photodiode to a predetermined voltage. However, Lee teaches a reset transistor (column 3, lines 35-36). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to

incorporate the teaching of Lee into the device taught by Tasumi and Kozlowski et al. in order to reduce the threshold voltage of the device.

Regarding claim 16, the combined device differs from the claimed invention by not showing a floating diffusion region, wherein the transistor is a transfer transistor for transferring charge from the photodiode to the floating diffusion region. However, Lee teaches a transfer transistor for transferring charge from the photodiode to the floating diffusion region (column 3, lines 36-38). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Lee into the device taught by Tasumi and Kozlowski et al. in order to increase the charge integrity of the photodiode.

Regarding claim 17, the combined device shows the photodiode is part of a CMOS image sensor (Lee; column 3, line 34).

Regarding claim 18, the combined device shows the photodiode is part of a charge coupled device image sensor (Lee; column 3, lines 34-40).

9. Claims 20-24 and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,818,322 to Tasumi in view of US Patent No. 6,762,401 to Lee and US Patent No. 6,127,692 to Sugawa et al.

Regarding claim 20, Tasumi (figures 1a-c) teaches an image sensor comprising:

the photodiode (superlattice structure [6]) comprising a plurality of layers, wherein at least a first layer comprises a first material and at least a second layer comprises a second material (superlattice structure [6] comprises alternating layers of Si and SiGe).

Tasumi differs from the claimed invention by not showing an array of pixel cells. However, Lee teaches a plurality of unit pixel arrayed in rows and columns (column 3, lines 18-21, lines 31-34). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Lee into the device taught by Tasumi in order to provide highly accurate imaging of the device.

The combined device shows a gate (Lee teaches the CMOS image sensor including a photodiode, a reset transistor for resetting the photodiode, and a transfer transistor for receiving an address signal and to transfer the charges from the photodiode to the floating diffusion region in a unit pixel; column 3, lines 31-38. Therefore, the gate is the portion of the transfer transistor, which receives an address signal and transfers the charges from the photodiode to the floating diffusion region in a unit pixel) adjacent to the photodiode for transferring the amplified charge from the photodiode.

Tasumi and Lee differ from the claimed invention by not showing the layers are configured such that a difference between the conduction band energies of the first and at least second materials and a difference between the valence band energies of the first and at least second materials promotes ionization by a first carrier type and suppresses ionization by a second carrier type. However, Sugawa et al. teach the layers are configured to promote and suppress ionization of the layers (column 21, lines 32-43). So, Sugawa et al. inherently teach the layers are configured such that a difference between the conduction band energies of the first and at least second materials and a difference between the valence band energies of the first and at least second materials for promotes ionization by a first carrier type and suppresses ionization by a second carrier type. Therefore, it would have been obvious to one having ordinary skill in the

art at the time the invention was made to incorporate the teaching of Sugawa et al. into the device taught by Tasumi and Lee in order to suppress the dark current in the layers.

Regarding claim 21, the combined device shows the first and at least second materials are selected from the group consisting of Si and SiGe (Tasumi; superlattice structure [6] has Si and SiGe layers).

Regarding claim 22, the combined device shows the first material is Si (Tasumi; Si layer of the superlattice structure [6]) and the second material is SiGe (Tasumi; SiGe layer of the superlattice structure [6]).

Regarding claim 23, the combined device shows the photodiode (Tasumi; superlattice structure [6]) comprises at least two layers of Si (Tasumi; 2 layers of Si of the superlattice structure [6]) and at least two layers of SiGe (Tasumi; 2 layers of SiGe of the superlattice structure [6]), wherein the layers of Si are doped to a first conductivity type, wherein the layers of SiGe are doped to a second conductivity type, and wherein the layers of Si are alternated with the layers of SiGe to form an Si/SiGe structure.

Regarding claim 24, the combined device shows the photodiode (Tasumi; superlattice structure [6]) comprises at least four layers of Si (Tasumi; 4 layers of Si of the superlattice structure [6]) and at least four layers of SiGe (Tasumi; 4 layers of SiGe of the superlattice structure [6]), wherein the layers of Si are alternated with the layers of SiGe to form an Si/SiGe structure, wherein at least a first subset of layers is doped to a first conductivity type, and wherein at least a second subset of layers is doped to a second conductivity type.

Regarding claim 27, the combined device shows the photodiode comprises approximately 10 to approximately 100 layers (Tasumi; superlattice structure [6] comprises 22 layers, which is in the range of the claimed invention).

Regarding claim 28, the combined device shows the transistor is a reset transistor (Lee; column 3, lines 35-36) for resetting the photodiode to a predetermined voltage.

Regarding claim 29, the combined device shows a floating diffusion region, wherein the transistor is a transfer transistor (Lee; column 3, lines 36-38) for transferring charge from the photodiode to the floating diffusion region.

Regarding claim 30, the combined device shows the pixel cell further comprises readout circuitry (Lee; driver transistor; column 3, lines 31-53) connected to a floating diffusion region for reading out charge (Lee; the charges transfer from the photodiode to the floating diffusion region in a unit pixel, a driver transistor coupled to each column of unit pixels, and display actual date obtained from the image data and the reference data).

10. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tasumi and Lee in view of Sugawa et al., and further in view of US Patent No. 6,403,975 to Brunner et al.

Regarding claim 25, the disclosures of Tasumi, Lee and Sugawa et al. are discussed as applied to claims 20-24 and 27-30 above.

The specification shows the value of x and y is $0 \leq (x \text{ or } y) \geq 1$ (page 10; paragraph [0046]). For instance, the value of $x = y = 0.5$, then the first layer of Si_xGe_{1-x} will be $Si_{0.5}Ge_{0.5}$ and the second layer of Si_yGe_{1-y} will be $Si_{0.5}Ge_{0.5}$.

The combined device differs from the claimed invention by not showing the first layer is Si_xGe_{1-x} (or $Si_{0.5}Ge_{0.5}$) and the second layer of Si_yGe_{1-y} (or $Si_{0.5}Ge_{0.5}$). However, Brunner et al. (figure 4c) teach the first layer of $Si_{1-x}Ge_x$ and the second layer of $Si_{1-x}Ge_x$ in the superlattice structure (alternating layers). Brunner et al. teach the value of x is in the range from 0.2 to 0.5 (column 8, lines 22-23), so the first layer of $Si_{1-x}Ge_x$ will be $Si_{0.5}Ge_{0.5}$ (when x is 0.5) and the second layer of $Si_{1-x}Ge_x$ will be $Si_{0.5}Ge_{0.5}$ (when x is 0.5). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Brunner et al. into the device taught by Tasumi, Lee and Sugawa et al. in order to provide highly sensitive to a longer wavelength of the device.

11. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tasumi and Lee in view of Sugawa et al., and further in view of US Patent No. 6,403,975 to Brunner et al. and US Patent No. 5,557,121 to Kozuka et al.

Regarding claim 26, the disclosures of Tasumi, Lee and Sugawa et al. are discussed as applied to claims 20-24 and 27-30 above.

The specification shows the value of x and y is $0 \leq (x \text{ or } y) \geq 1$ (page 10; paragraph [0046]). For instance, the value of $x = 0.5$ and $y = 0$, then the first layer of $Si_xGe_{1-x}C_y$ will be $Si_{0.5}Ge_{0.5}$

The combined device differs from the claimed invention by not showing the first layer is $Si_xGe_{1-x}C_y$ (or $Si_{0.5}Ge_{0.5}$). However, Brunner et al. (figure 3a) teach the first layer of $Si_{1-x-y}Ge_xC_y$ in the superlattice structure (alternating layers). Brunner et al. teach the value of x is in the range from 0 to 0.5 and y is in the range from 0 to 0.1 (column 8, lines 19-20), so the first layer of Si_{1-x-}

$_yGe_xC_y$ will be $Si_{0.5}Ge_{0.5}$ (when x = 0.5 and y = 0). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Brunner et al. into the device taught by Tasumi, Lee and Sugawa et al. in order to provide the long wavelength light of the device.

The combined device differs from the claimed invention by not showing the second layer is $Si_xGe_yC_z$. However, Kozuka et al. teach the layer of $Si_xGe_yC_z$ (column 5, lines 53-54). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Kozuka et al. into the device taught by Tasumi, Lee, Sugawa et al. and Brunner et al. in order to provide the long wavelength light of the device.

12. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tasumi and Lee in view of Sugawa et al., and further in view of US Patent Application Publication No. 2003/0218678 to Lin et al.

Regarding claim 31, the disclosures of Tasumi, Lee and Sugawa et al. are discussed as applied to claims 20-24 and 27-30 above.

The combined device shows the substrate is a silicon-on-insulator substrate (Tasumi; column 4, lines 19-22).

The combined device differs from the claimed invention by not showing circuitry peripheral to the array, the peripheral circuitry being at a surface of the substrate. However, Lin et al. teach a pixel array (16) and the peripheral circuit (12, 14) (column 3, paragraph [0030]). Therefore, it would have been obvious to one having ordinary skill in the art at the time the

invention was made to incorporate the teaching of Lin et al. into the device taught by Tasumi, Lee and Sugawa et al. in order to provide high performance logic transistor of the device.

13. Claims 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,818,322 to Tasumi in view of US Patent No. 6,762,401 to Lee and US Patent No. 6,403,975 to Brunner et al.

Regarding claim 32, Tasumi (figures 1a-c) teaches an image sensor comprising:

the photodiode (superlattice structure [6] comprises alternating layers of Si and SiGe) comprising alternating layers.

Tasumi differs from the claimed invention by not showing an array of pixel cells. However, Lee teaches a plurality of unit pixel arrayed in rows and columns (column 3, lines 18-30). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Lee into the device taught by Tasumi in order to provide highly accurate imaging of the device.

The combined device shows a gate (Lee teaches the CMOS image sensor including a photodiode, a reset transistor for resetting the photodiode, and a transfer transistor for receiving an address signal and to transfer the charges from the photodiode to the floating diffusion region in a unit pixel; column 3, lines 31-38. Therefore, the gate is the portion of the transfer transistor, which receives an address signal and transfers the charges from the photodiode to the floating diffusion region in a unit pixel) adjacent to the photodiode for transferring the amplified charge from the photodiode.

The specification shows the value of x and y is $0 \leq (x \text{ or } y) \geq 1$ (page 10; paragraph [0046]). For instance, the value of $x = 0.5$, then the layer of Si_xGe_{1-x} will be $Si_{0.5}Ge_{0.5}$.

The combined device shows the photodiode comprising alternating layers of Si and SiGe (Tasumi; superlattice structure [6] comprising alternating layers of Si and SiGe). So, the first layer of alternating layers is Si. The combined device differs from the claimed invention by not showing the second layer of the alternating layers, which is Si_xGe_{1-x} (or $Si_{0.5}Ge_{0.5}$). However, Brunner et al. (figure 4c) teach layer of $Si_{1-x}Ge_x$ in the superlattice structure (alternating layers). Brunner et al. teach the value of x is in the range from 0.2 to 0.5 (column 8, lines 22-23), so the layer of $Si_{1-x}Ge_x$ will be $Si_{0.5}Ge_{0.5}$ (when x is 0.5). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Brunner et al. into the device taught by Tasumi and Lee in order to provide highly sensitive to a longer wavelength of the device.

Regarding claim 33, the combined device shows x is approximately 0.5 (Brunner et al.; the value of x is in the range from 0.2 to 0.5; column 8, lines 22-23), wherein the layers of Si (Tasumi; layer Si is in the superlattice structure [6]) are doped to a first conductivity type, and wherein the layers of Si_xGe_{1-x} (Brunner et al.) are doped to a second conductivity type.

Regarding claim 34, the combined device shows x is approximately 0.5 (Brunner et al.; the value of x is in the range from 0.2 to 0.5; column 8, lines 22-23), and wherein first (Tasumi; layer Si of the superlattice structure [6]) and at least second (Brunner et al.; $Si_{0.5}Ge_{0.5}$ layer when x is 0.5) subsets of the layers are doped to first conductivity and second conductivity types, respectively.

14. Claims 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,762,401 to Lee in view of US Patent No. 6,462,365 to He et al., US Patent No. 6,403,975 to Brunner et al. and US Patent No. 6,127,692 to Sugawa et al.

Regarding claim 35, Lee teaches the image sensor comprising:

an array of pixel cells (column 3, lines 18-30), at least one of the pixel cells comprising a photodiode (column 3, lines 31-34);

a gate of a transistor (Lee teaches the CMOS image sensor including a photodiode, a reset transistor for resetting the photodiode, and a transfer transistor for receiving an address signal and to transfer the charges from the photodiode to the floating diffusion region in a unit pixel; column 3, lines 31-38. Therefore, the gate is the portion of the transfer transistor, which receives an address signal and transfers the charges from the photodiode to the floating diffusion region in a unit pixel) adjacent to the photodiode;

a floating diffusion region electrically connected to the first transistor (Lee teaches a transfer transistor receives signal and transfers the charges from the photodiode to the floating diffusion region in a unit pixel; column 3, lines 31-38. Therefore, the transfer transistor of Lee electrically connected to the floating diffusion region for receiving and transferring the charges from the photodiode); and

readout circuitry electrically connected to the floating diffusion region (Lee teaches storing an output voltage of the floating diffusion region into a register assigned from the column as image data through the driver transistor and displaying actual data obtained from the image data; column 3, lines 31-53. Therefore, the driver transistor of Lee is the readout circuitry

electrically connected to the floating diffusion region for displaying the image data of the image sensor device).

Lee differs from the claimed invention by not showing a processor and an image sensor coupled to the processor. However, He et al. (figure 10) teach a processor (1105) and an image sensor (1103) coupled to the processor (1105) (column 5, lines 29-37). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of He et al. into the device taught by Lee because the image sensor and the processor will be manufactured in a standard CMOS processes.

The specification shows the value of x and y is $0 \leq (x \text{ or } y) \geq 1$ (page 10; paragraph [0046]). For instance, the value of $x = 0.5$, then one of the second layer of Si_xGe_{1-x} will be $Si_{0.5}Ge_{0.5}$.

Lee differs from the claimed invention by not showing the photodiode comprising layers of a first material and at least a second material in contact with one another, wherein the first and second materials are selected from Si and Si_xGe_{1-x} (or $Si_{0.5}Ge_{0.5}$). However, Brunner et al. (figure 4a) teach the first layer of Si (15) and the second layer of $Si_{1-x-y}Ge_xC_y$ (14) in the superlattice structure (alternating layers). Brunner et al. teach the value of x is in the range from 0 to 0.5 and y in the range from 0 to 0.1 (column 8, lines 19-20), so the first layer is Si and the second layer of $Si_{1-x-y}Ge_xC_y$ will be $Si_{0.5}Ge_{0.5}$ (when $x = 0.5$ and $y = 0$). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Brunner et al. into the device taught by Lee in order to provide highly sensitive to a longer wavelength of the device.

Lee and Brunner et al. differ from the claimed invention by not showing the layers are configured to promote ionization by a first carrier type and suppress ionization by a second carrier type. However, Sugawa et al. teach the layers are configured to promote and suppress ionization of the layers (column 21, lines 32-36). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sugawa et al. into the device taught by Lee and Brunner et al. in order to suppress the dark current in the layers.

Regarding claim 36, the combined device shows the first layer and second layer (Brunner et al.; superlattice structure comprises alternating layers of Si and $Si_{1-x-y}Ge_xC_y$), which are Si and $Si_{1-x-y}Ge_xC_y$ (or $Si_{0.5}Ge_{0.5}$), the same material as the instant invention (Si and Si_xGe_{1-x} [or $Si_{0.5}Ge_{0.5}$]). Therefore, the first and second layers of Brunner et al. have a difference between the conduction band energies of the first layer and the second layer is greater than a difference between the valence band energies of the first layer and the second layer, which reduce the dark current and minimize the noise between the first layer and the second layer.

Regarding claim 37, the combined device shows the first layer and second layer (Brunner et al.; superlattice structure comprises alternating layers of Si and $Si_{1-x-y}Ge_xC_y$), which are Si and $Si_{1-x-y}Ge_xC_y$ (or $Si_{0.5}Ge_{0.5}$), the same material as the instant invention (Si and Si_xGe_{1-x} [or $Si_{0:5}Ge_{0.5}$]). Therefore, the first and second layers of Tasumi have a difference between the valence band energies of the first layer and the second layer is greater than a difference between the conduction band energies of the first layer and the a second layer, which suppress the impact of the ionization between the first and second material layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D. Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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